Notice of Allowability	Application No.	Applicant(s)	
	10/039,233	CASSAGNES, HERVE	
	Examiner	Art Unit	
	Phuong Phu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed on 7/24/07*.

2. ☒ The allowed claim(s) is/are *13,16-24,26-30 and 32-35*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 7/24/07. Accordingly, claims 13, 16-24, 26-30 and 32-35 are currently pending; and claims 1-12, 14, 15, 25 and 31 are canceled.

REASONS FOR ALLOWANCE

2. Claims 13, 16-24, 26-30 and 32-35 are allowed.

3. The following is an examiner's statement of reasons for allowance:

-Regarding independent claim 13, none of prior art of record teaches or suggests a decoding circuit for decoding a biphase signal having a pair of states, as claimed. Hiramatsu teaches the claimed decoding circuit except he at least fails to teach a precharging register and verification circuit, wherein in light of the specification figures 2 and 3 and pages 7-9, the precharging register is a 4-bit shift register having four D type latches series connected, and in operation, the precharging register precharges respective states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal in such a way that at each active edge of the periodic precharging signal, a state of the biphase signal entered as a least significant bit into the precharging register, and the four bits appeared at respective outputs of the four D type latches of the precharging register are given as the precharging register's parallel output for further being inputted into and compared by the verification circuit. It would not have been obvious for one skilled in the art to implement Hiramatsu in view of other prior art for leading such the implementation to the claimed invention.

-Regarding independent claim 19, none of prior art of record teaches or suggests a decoding circuit for decoding a biphase signal having a pair of states, as claimed. Hiramatsu

teaches the claimed decoding circuit except he at least fails to teach a precharging register and verification circuit, wherein in light of the specification figures 2 and 3 and pages 7-9, the precharging register is a 4-bit shift register having four D type latches series connected, and in operation, the precharging register precharges respective states of the biphase signal, one state of the pair of states being precharged at each pulse of a periodic precharging signal in such a way that at each active edge of the periodic precharging signal, a state of the biphase signal entered as a least significant bit into the precharging register, and the four bits appeared at respective outputs of the four D type latches of the precharging register are given as the precharging register's parallel output for further being inputted into and compared by the verification circuit. It would not have been obvious for one skilled in the art to implement Hiramatsu in view of other prior art for leading such the implementation to the claimed invention.

-Regarding independent claim 23, none of prior art of record teaches or suggests a circuit for transmitting and receiving biphase signals having respective pairs of states, as claimed. Hiramatsu teaches the claimed circuit except he at least fails to teach a precharging register and verification circuit, wherein in light of the specification figures 2 and 3 and pages 7-9, the precharging register is a 4-bit shift register having four D type latches series connected, and in operation, the precharging register precharges respective states of the biphase signals, one state of each pair of states being precharged at each pulse of a periodic precharging signal in such a way that at each active edge of the periodic precharging signal, a state of a respective biphase signal entered as a least significant bit into the precharging register, and the four bits appeared at respective outputs of the four D type latches of the precharging register are given as the precharging register's parallel ouput for further being inputted into and compared by the

verification circuit. It would not have been obvious for one skilled in the art to implement Hiramatsu in view of other prior art for leading such the implementation to the claimed invention.

-Regarding independent claim 30, none of prior art of record teaches or suggests a method for decoding a a biphase signal having a pair of states, as claimed. Hiramatsu teaches the claimed decoding method except he at least fails to teach a precharging procedure associated with a precharging register and a comparing procedure, wherein in light of the specification figures 2 and 3 and pages 7-9, in the precharging procedure, the charging register is a 4-bit shift register having four D type latches series connected, and in operation, the precharging register precharges one of the pair of states of the biphase signal at each pulse of a periodic precharging signal in such a way that at each active edge of the periodic precharging signal, a state of the biphase signal entered as a least significant bit into the precharging register, and the four bits appeared at respective outputs of the four D type latches of the precharging register are given as the precharging register's parallel output for a further comparison via the comparing procedure. It would not have been obvious for one skilled in the art to implement Hiramatsu in view of other prior art for leading such the implementation to the claimed invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu
Primary Examiner
Art Unit 2611

Phuong Phu
08/31/07

PHUONG PHU
PRIMARY EXAMINER